What is claimed is:

1. A packet transfer device comprising:

a plurality of input/output ports;

a header information extracting circuit for extracting header information belonging to a 3rd layer and higher layers of a network protocol from packets inputted from the respective input/output ports;

a table storing header information and control information corresponding to the header information in association with each other;

a control information acquiring circuit for acquiring control information corresponding to the header information extracted by said header information extracting circuit from the table; and

a processing circuit for processing packets based on the control information acquired by said control information acquiring circuit.

2. A packet transfer device according to claim 1, wherein said control information represents whether a filtering process is to be effected on a packet or not, and said processing circuit discards the packet if said control information indicates that the filtering process is to be effected on the packet.

3. A packet transfer device according to claim 2, further comprising an input/output port connected to an external network, wherein said processing circuit filters a packet inputted from the input/output port connected to the external network if the packet has address information of an internal unit thereof.

4. A packet transfer device according to claim 1, wherein said control information represents either one of said input/output ports from which to output the packet, and said processing circuit outputs the packet from the input/output port represented by said control information.

5. A packet transfer device according to claim 1, wherein said table stores a plurality of items of header information belonging to different layers and control information corresponding to the items of header information.

6. A packet transfer device according to claim 1, further comprising a plurality of tables storing different items of information.

7. A packet transfer device according to claim 1, further comprising a process determining circuit for determining a process to be actually performed by said processing circuit if a plurality of items of control in-

formation are acquired from a plurality of tables with respect to one packet by said control information acquiring circuit.

8. A packet transfer device according to claim 7, wherein said control information represents whether a filtering process is to be effected on a packet or not, and said process determining circuit discards the packet if the items of control information are acquired from said tables and either one of the acquired items of control information indicates that the filtering process is to be effected on the packet.

9. A packet transfer device according to claim 7, wherein said control information represents either one of said input/output ports from which to output the packet, and said process determining circuit outputs the packet from the input/output port represented by the control information acquired from the table containing header information belonging to a highest layer if the items of control information are acquired from said tables.

10. A packet transfer device according to claim 7, wherein said control information includes information representing either one of said input/output ports from which to output the packet and information representing whether a filtering process is to be effected on a packet

or not, and said process determining circuit discards the packet if both the information representing either one of said input/output ports from which to output the packet and the information representing whether the filtering process is to be effected on the packet or not are acquired from said tables.

11. A packet transfer device according to claim 1, further comprising a routing processing circuit for performing a routing process.

12. A packet transfer device according to claim 1, further comprising a table rewriting circuit for rewriting the information stored in said table.

13. A packet transfer device according to claim 1, wherein said control information represents the priority of a packet, and said processing circuit processes the packet according to the priority represented by said control information.

14. A packet transfer device according to claim 1, further comprising a storage circuit for temporarily storing a packet, wherein said processing circuit writes, reads, and transmits the packet stored in said storage circuit based on the priority thereof.

15. A semiconductor device comprising:

a plurality of input/output ports;

a header information extracting circuit for extracting header information belonging to a 3rd layer and higher layers of a network protocol from packets inputted from the respective input/output ports;

a table storing header information and control information corresponding to the header information in association with each other;

a control information acquiring circuit for acquiring control information corresponding to the header information extracted by said header information extracting circuit from the table; and

a processing circuit for processing packets based on the control information acquired by said control information acquiring circuit.

16. A packet transfer system for transferring packets between a plurality of networks connected by a packet transfer device, said packet transfer device comprising:

a plurality of input/output ports;

a header information extracting circuit for extracting header information belonging to a 3rd layer and higher layers of a network protocol from packets inputted from the respective input/output ports;

a table storing header information and control information corresponding to the header information in association with each other;

a control information acquiring circuit for acquiring control information corresponding to the header information extracted by said header information extracting circuit from the table; and

a processing circuit for processing packets based on the control information acquired by said control information acquiring circuit.